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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,079	10/31/2003	Manolito M. Catalasan	1875.4360002	9730

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EXAMINER	
TRINH, HOA B	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,079	CATALASAN ET AL.	
	Examiner	Art Unit	
	Vikki H. Trinh	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-9 and 15-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/24/05, 01/10/05*, 12/29/04, 04/20/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of a Species directed to claims 10-14 in the reply filed on 10/24/05 is acknowledged.

Applicants argue that claims 10-14 are directed to species VI-V of figures 6-7D because they relate to the same species. This is found persuasive. Thus, the examiner will examine in this Office Action, Species VI-V, claims 10-14.

2. Claims 1-9 and 15-24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 10/24/05.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 10-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Burgess et al. (5,408,428) (hereinafter Burgess).

As to claim 10, Burgess discloses an integrated circuit chip including a plurality of metal layers M1-M4 (fig. 3) and first and second supply potentials 28 VDD, 26 GND, respectively (fig.

9), a programmable memory cell 16 (fig. 3) for storing a value, the memory cell comprising a first metal interconnect structure 30 (fig. 3) that traverses the plurality of metal layers using a first 32 plurality of vias 32, 36, 44, 40, 48, 52 (fig. 3); a second metal interconnect structure 38 (fig. 3) that traverses the plurality of metal layers using a second 38 plurality of vias (fig. 3), an output 56 Vout (fig. 3) coupled to one of the first and second supply potentials by at least one of said first and second metal interconnect structure, wherein each of said first and second metal interconnect structures can be programmed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers (figs. 3-7).

As to claim 12, one of said first and second metal interconnect structures (fig. 3) is coupled to the first supply potential VDD at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential GND at the bottom metal layer (fig. 3).

As to claim 13, the interconnect structures form a ladder structure (fig. 3).

As to claim 14, the interconnect structures form an offset ladder structure (fig. 7).

5. Claims 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Bansal (6,765,245).

As to claim 10, Bansal discloses an integrated circuit chip including a plurality of metal layers M1-M5 (col. 3, lines 8-1) and first and second supply potentials VDD, GND, respectively (fig. 9), a programmable memory cell (fig. 3) for storing a value, the memory cell comprising a first metal interconnect structure 5 (fig. 9) that traverses the plurality of metal layers using a first plurality of vias; a second metal interconnect structure 6 (fig. 9) that traverses the plurality of metal layers using a second plurality of vias (fig. 9), an output (fig. 9) coupled to one of the first

and second supply potentials by at least one of said first and second metal interconnect structure, wherein each of said first and second metal interconnect structures can be programmed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers.

As to claim 11, the first and second metal interconnect structures 5, 6 (fig. 9) are not electrically coupled to each other at a top metal layer thereby forming two outputs for the memory cell.

As to claim 12, one of said first and second metal interconnect structures 5,6 (fig. 9) is coupled to the first supply potential VDD at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential GND at the bottom metal layer (fig. 9).

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 10, 12-14 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 9, 14-16, 18-20, 30 of U.S. Patent No. 6,933,547. Although the conflicting claims are not identical, they are not patentably distinct from each other because they claim substantially similar subject matter.

Claims 1, 14-16, 18, 20, of Patent '547 discloses an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a programmable memory cell (line 3) for storing a value, the memory cell comprising a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias; a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, an output Vout coupled to one of the first and second supply potentials by at least one of said first and second metal interconnect structure, wherein each of said first and second metal interconnect structures can be programmed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers.

Claim 30 of Patent '547 states that one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer .

Claims 9, 19, of the Patent '547 states that the interconnect structures form a ladder structure .

As to claim 20 of the Patent '547, the interconnect structures form an offset ladder structure .

8.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests

to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

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HOWARD WEISS
PRIMARY EXAMINER